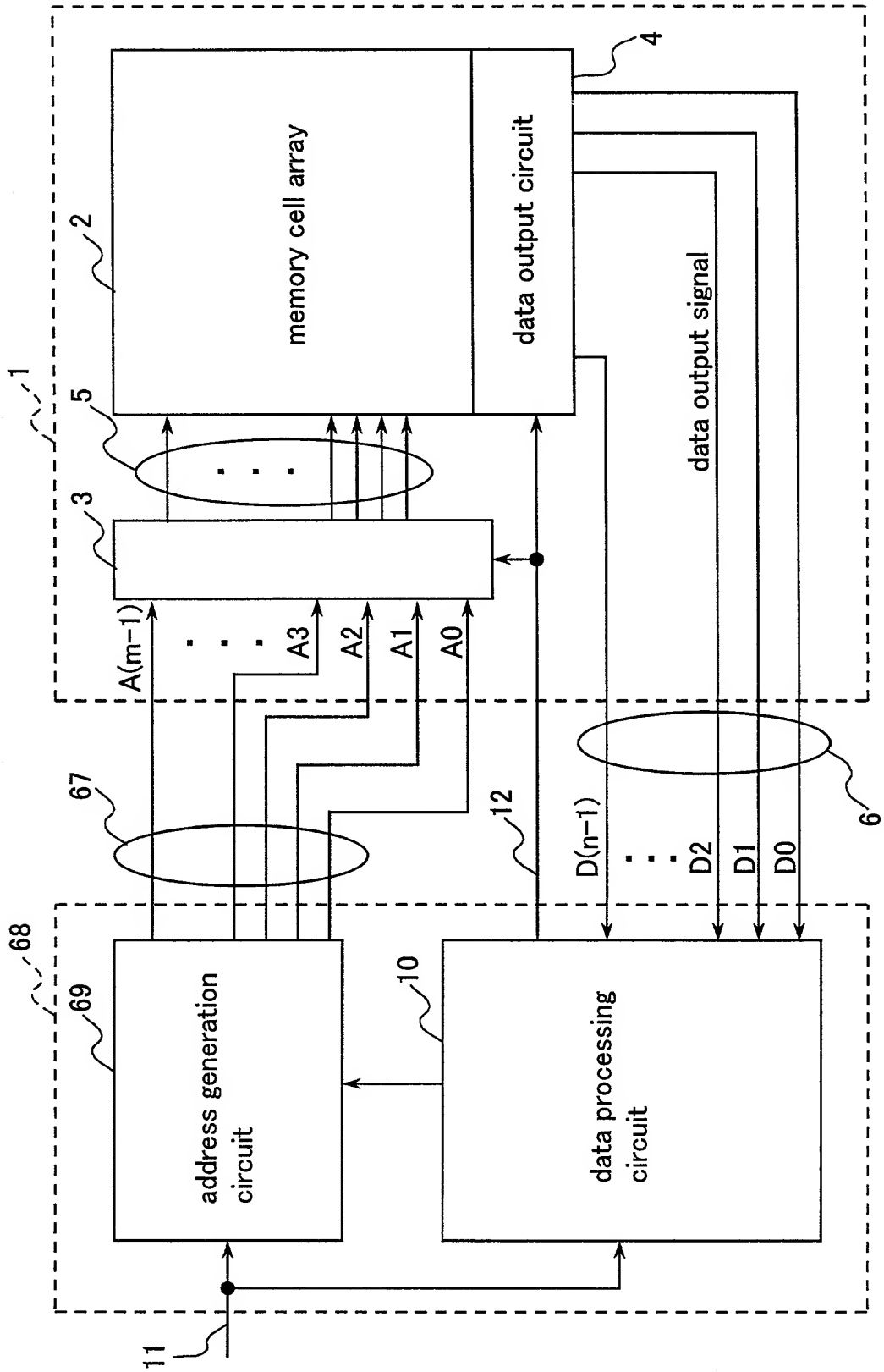

memory cell array
data output circuit
data output signal
address generation circuit
data processing circuit
A(m−1)
A3
A2
A1
A0
D(n−1)
D2
D1
D0
1
2
3
4
5
6
10
11
12
67
68
69

FIG. 1

FIG. 2A

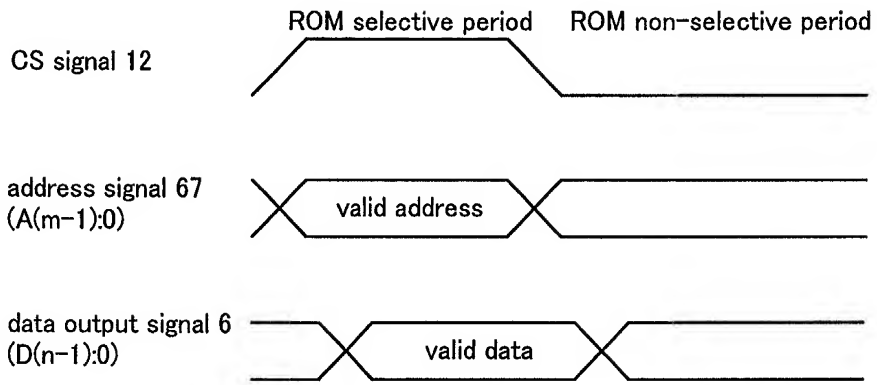
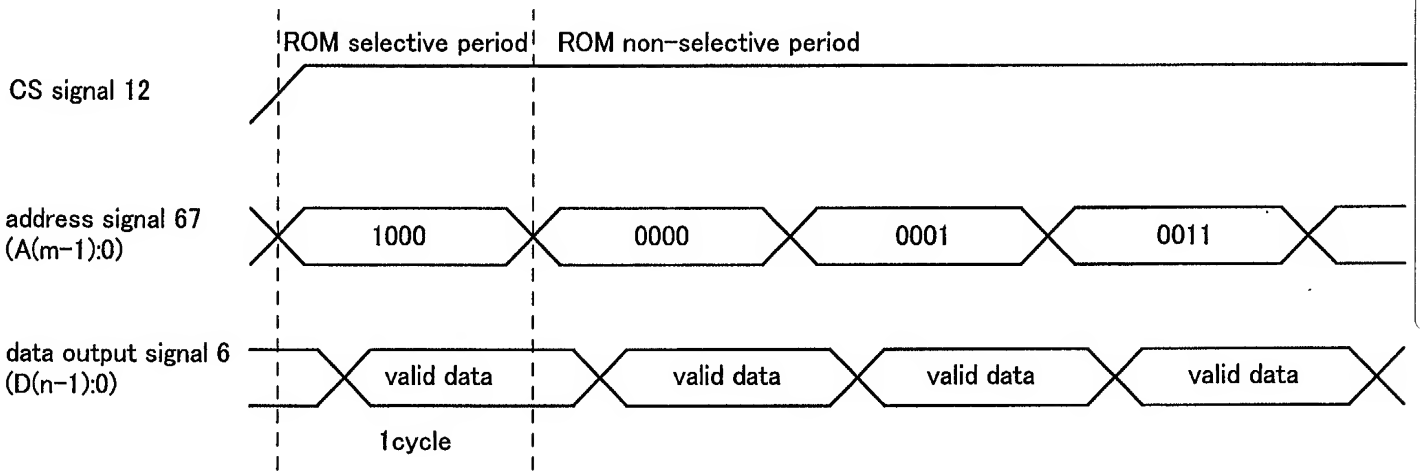


FIG. 2B



A3	A2	A1	A0	a number of changing bits
0	0	0	0	1
0	0	0	1	1
0	0	1	1	1
0	0	1	0	1
0	1	1	0	1
0	1	1	1	1
0	1	0	1	1
0	1	0	0	1
1	1	0	0	1
1	1	0	1	1
1	1	1	1	1
1	1	1	0	1
1	0	1	0	1
1	0	1	1	1
1	0	0	1	1
1	0	0	0	1
				total 16

FIG. 3

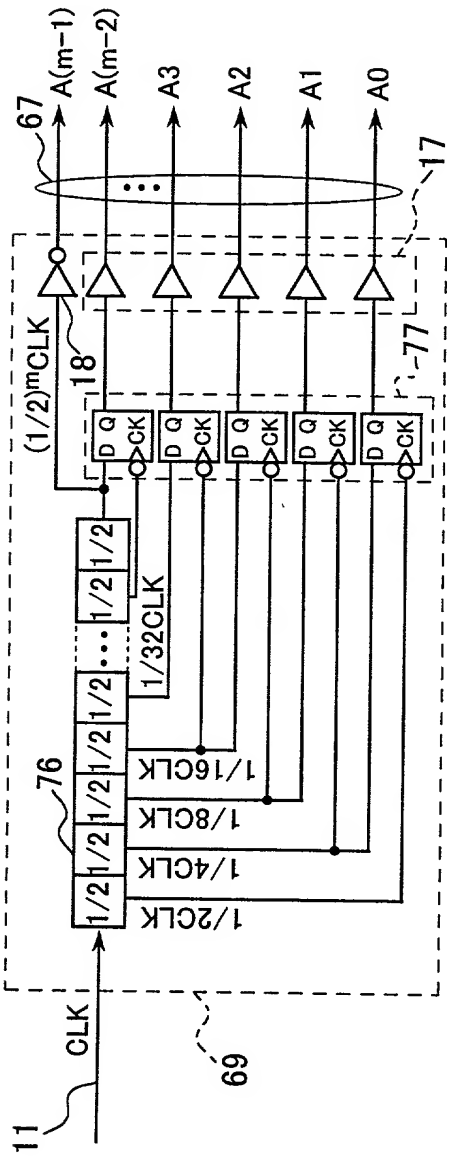

67
A(m-1)
A(m-2)
A3
A2
A1
A0
17
(1/2)^mCLK
18
77
D Q
CK
1/2
1/32CLK
1/16CLK
1/8CLK
1/4CLK
1/2CLK
76
CLK
11
69

FIG. 4A

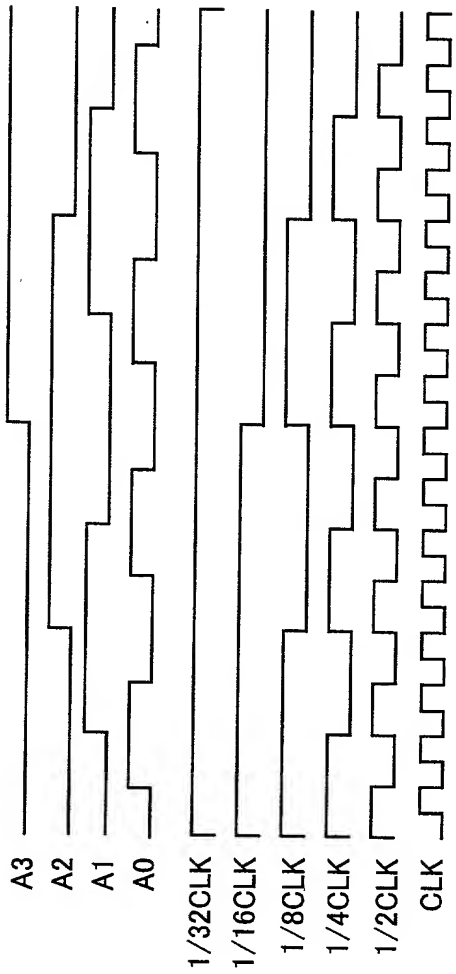

A3
A2
A1
A0
1/32CLK
1/16CLK
1/8CLK
1/4CLK
1/2CLK
CLK

FIG. 4B

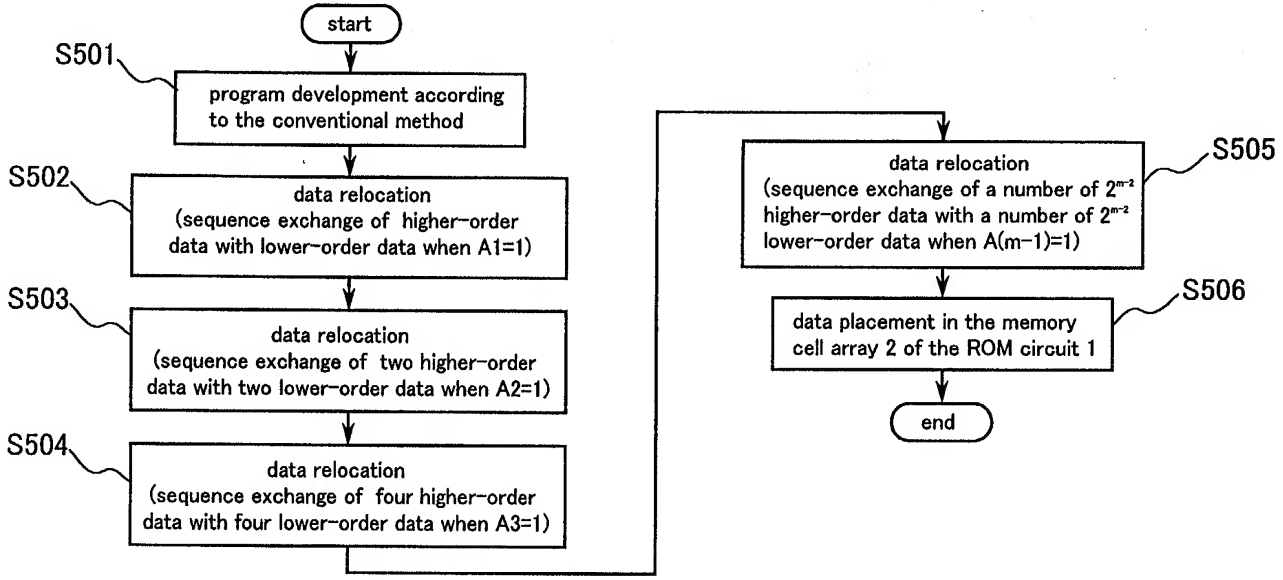


FIG. 5A

when program is developed

A3	A2	A1	A0	when data are created	relocation (A1=1)	relocation (A2=1)	relocation (A3=1)
0	0	0	0	table data 0	table data 0	table data 0	table data 0
0	0	0	1	table data 1	table data 1	table data 1	table data 1
0	0	1	0	table data 2	table data 3	table data 3	table data 3
0	0	1	1	table data 3	table data 2	table data 2	table data 2
0	1	0	0	table data 4	table data 4	table data 7	table data 7
0	1	0	1	table data 5	table data 5	table data 6	table data 6
0	1	1	0	table data 6	table data 7	table data 4	table data 4
0	1	1	1	table data 7	table data 6	table data 5	table data 6
1	0	0	0	instruction data 0	instruction data 0	instruction data 0	instruction data 7
1	0	0	1	instruction data 1	instruction data 1	instruction data 1	instruction data 6
1	0	1	0	instruction data 2	instruction data 3	instruction data 3	instruction data 4
1	0	1	1	instruction data 3	instruction data 2	instruction data 2	instruction data 5
1	1	0	0	instruction data 4	instruction data 4	instruction data 7	instruction data 0
1	1	0	1	instruction data 5	instruction data 5	instruction data 6	instruction data 1
1	1	1	0	instruction data 6	instruction data 7	instruction data 4	instruction data 3
1	1	1	1	instruction data 7	instruction data 6	instruction data 5	instruction data 2

programs to be processed in sequence

FIG. 5B

when program is executed

A3	A2	A1	A0	data
0	0	0	0	table data 0
0	0	0	1	table data 1
0	0	1	1	table data 2
0	0	1	0	table data 3
0	1	1	0	table data 4
0	1	1	1	table data 5
0	1	0	1	table data 6
0	1	0	0	table data 7
1	1	0	0	instruction data 0
1	1	0	1	instruction data 1
1	1	1	1	instruction data 2
1	1	1	0	instruction data 3
1	0	1	0	instruction data 4
1	0	1	1	instruction data 5
1	0	0	1	instruction data 6
1	0	0	0	instruction data 7

FIG. 5C

FIG. 6A

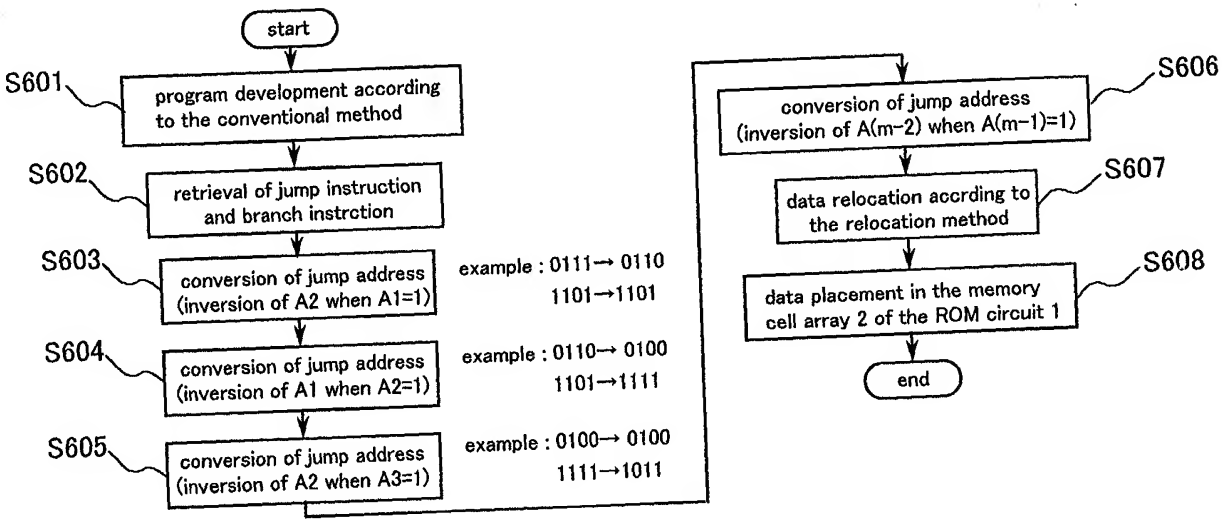


FIG. 6B

when program is developed

A3	A2	A1	A0	data
0	0	0	0	instruction data 0
0	0	0	1	instruction data 1
0	0	1	0	JUMP
0	0	1	1	address 0111
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	instruction data 2
1	0	0	0	BRA
1	0	0	1	address 1101
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	instruction data 0
1	1	1	0	instruction data 1
1	1	1	1	instruction data 2

jump to address 0111 → jump to address 0100

branch to address 1101 → branch to address 1011

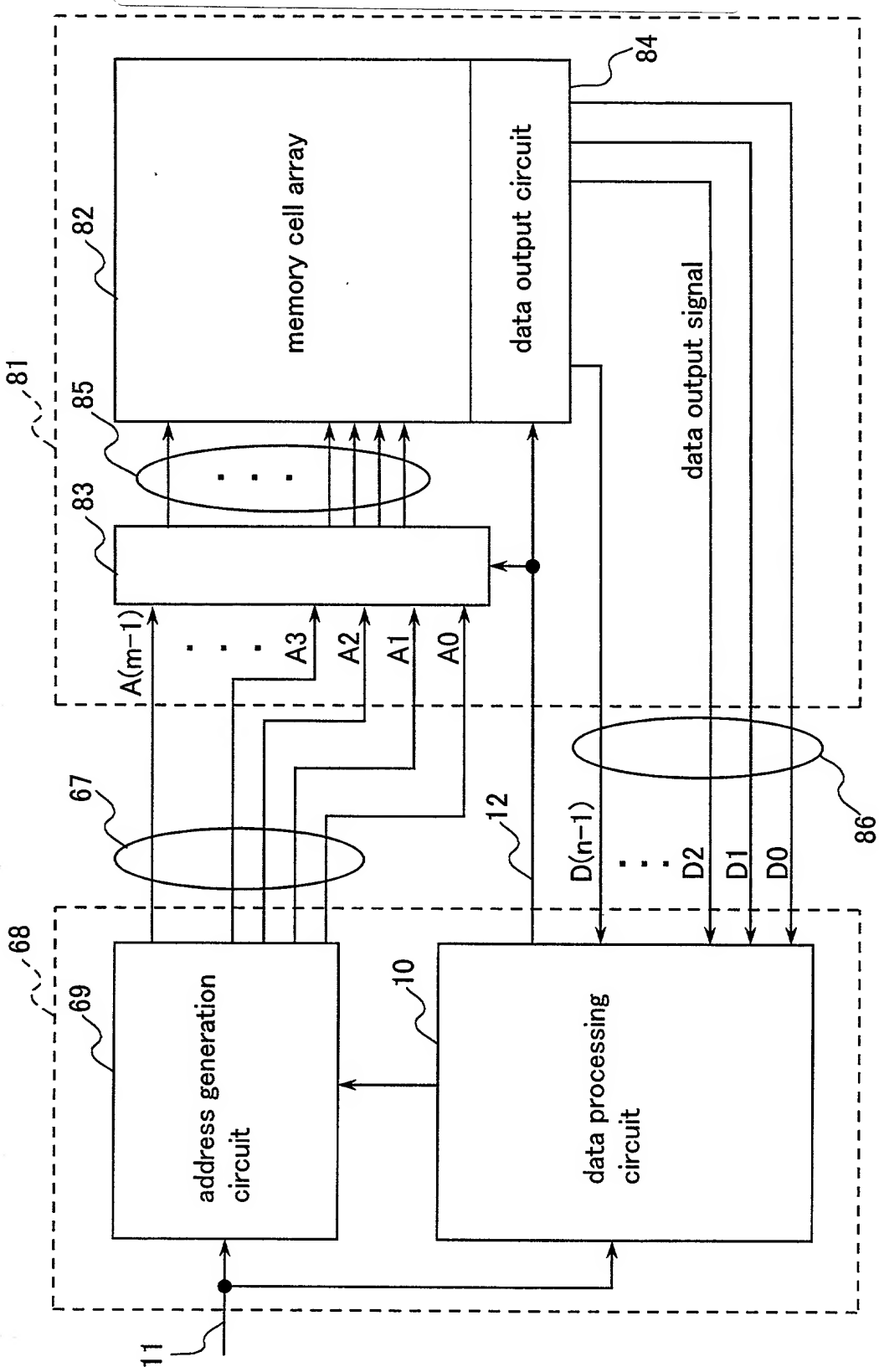

81
82
memory cell array
84
data output circuit
data output signal
85
83
A(m−1)
A3
A2
A1
A0
67
12
D(n−1)
D2
D1
D0
86
68
69
address generation circuit
10
data processing circuit
11

FIG. 7

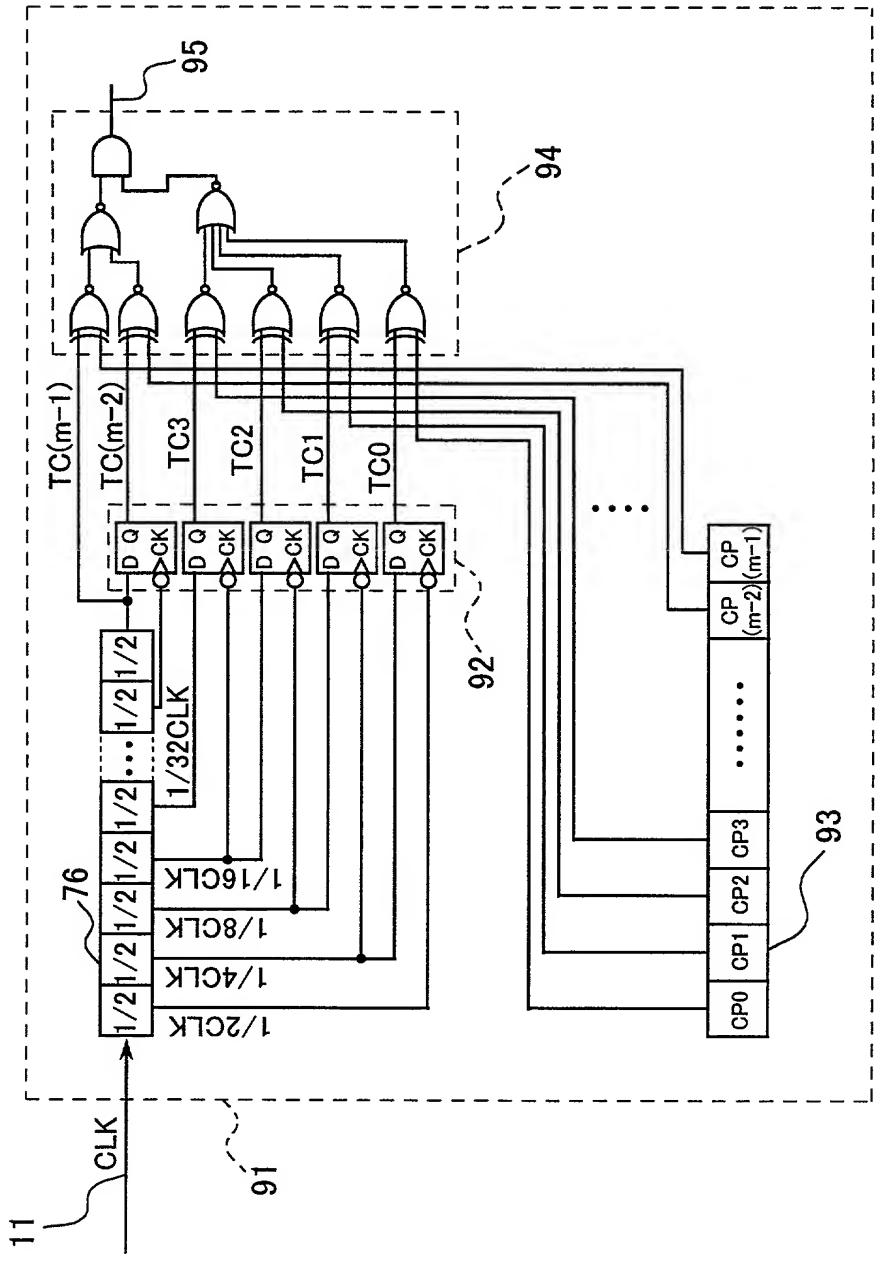

95
94
TC(m-1)
TC(m-2)
TC3
TC2
TC1
TC0
D Q CK
92
1/2
1/32CLK
1/16CLK
1/8CLK
1/4CLK
1/2CLK
76
CP(m-1)
CP(m-2)
CP3
CP2
CP1
CP0
93
CLK
11
91

FIG. 8

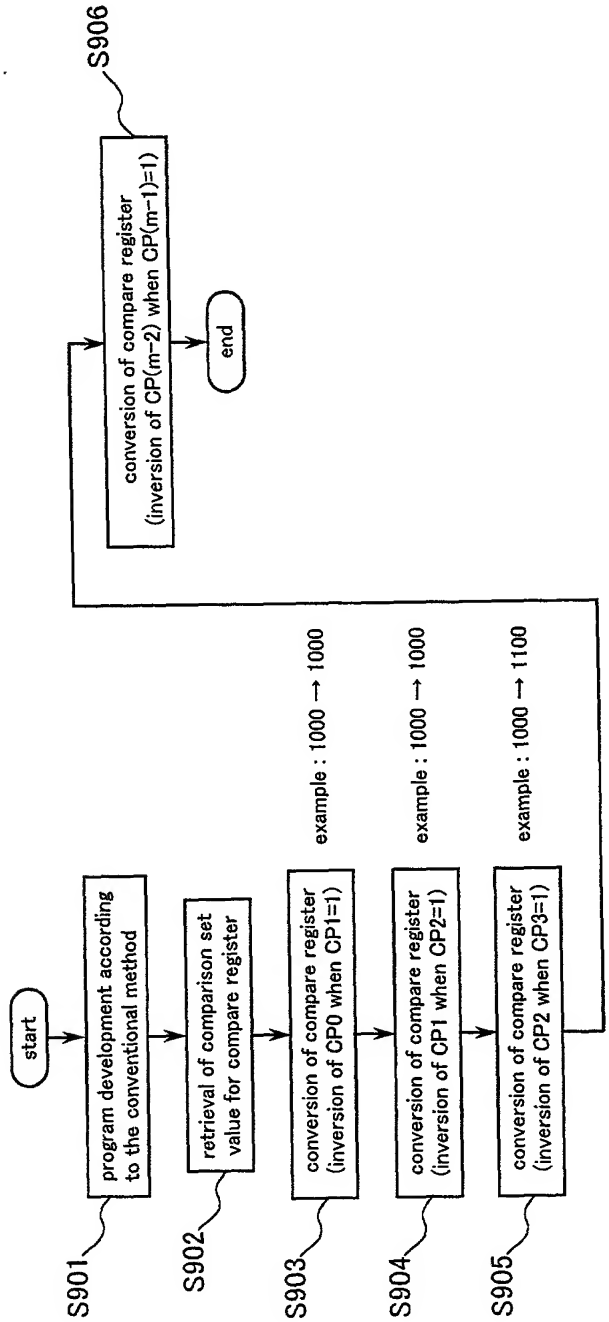

start
program development according to the conventional method
retrieval of comparison set value for compare register
conversion of compare register (inversion of CP0 when CP1=1)
conversion of compare register (inversion of CP1 when CP2=1)
conversion of compare register (inversion of CP2 when CP3=1)
example : 1000 → 1000
example : 1000 → 1000
example : 1000 → 1100
conversion of compare register (inversion of CP(m−2) when CP(m−1)=1)
end
S901
S902
S903
S904
S905
S906

FIG. 9

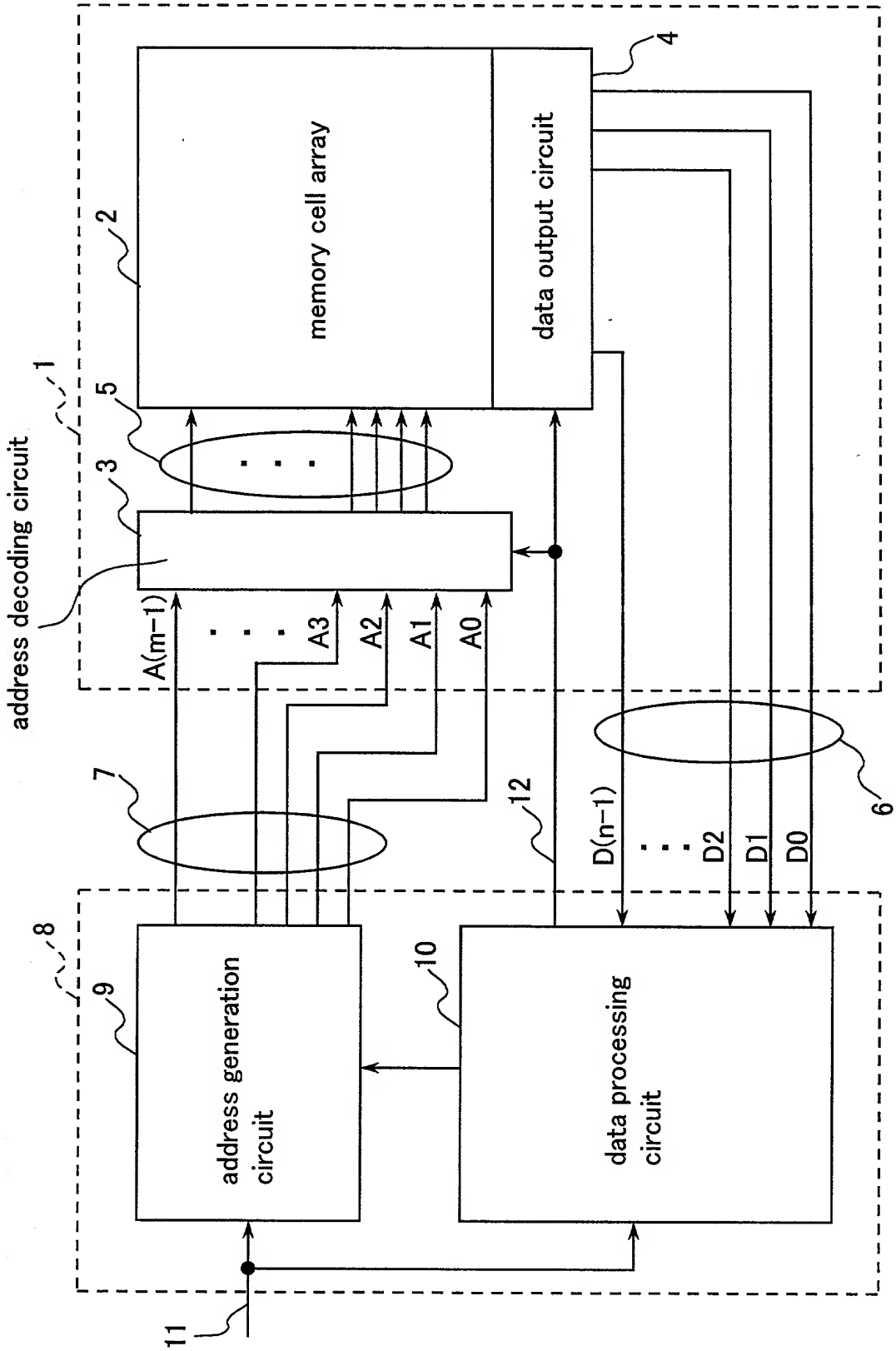


FIG. 10 (PRIOR ART)

FIG. 11A
(PRIOR ART)

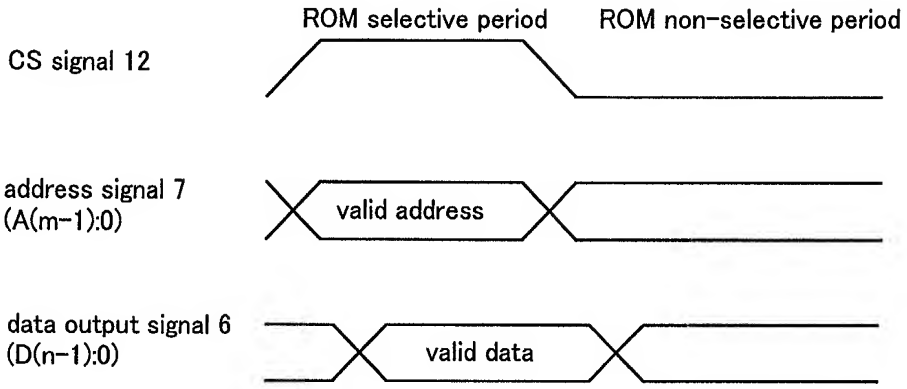
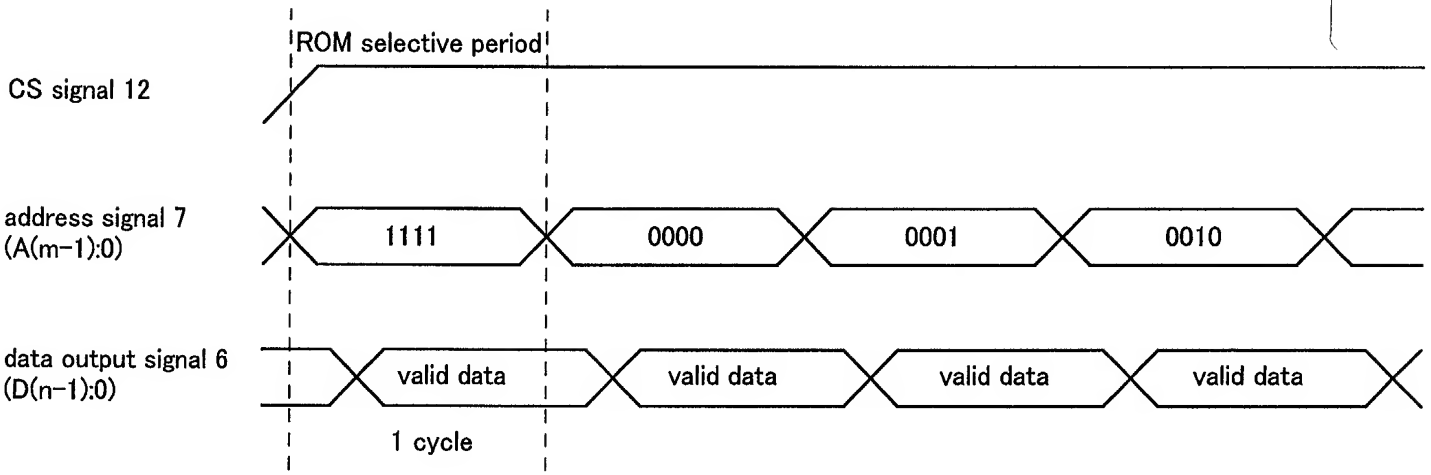


FIG. 11B
(PRIOR ART)



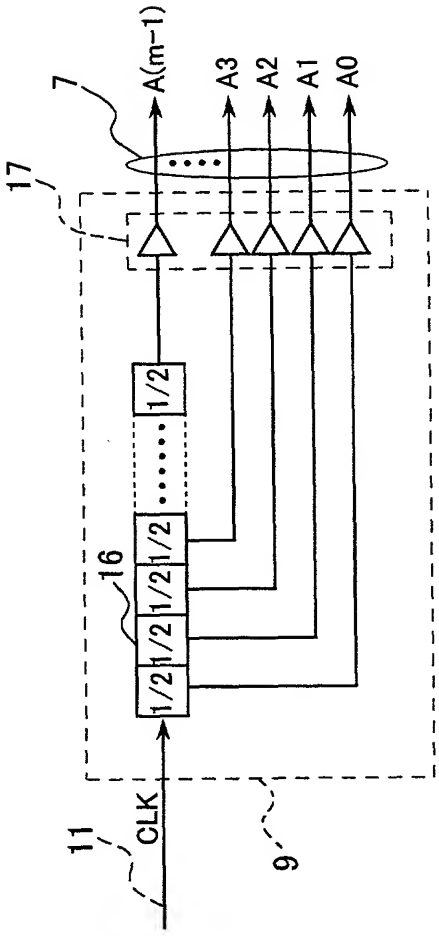


FIG. 12A
(PRIOR ART)

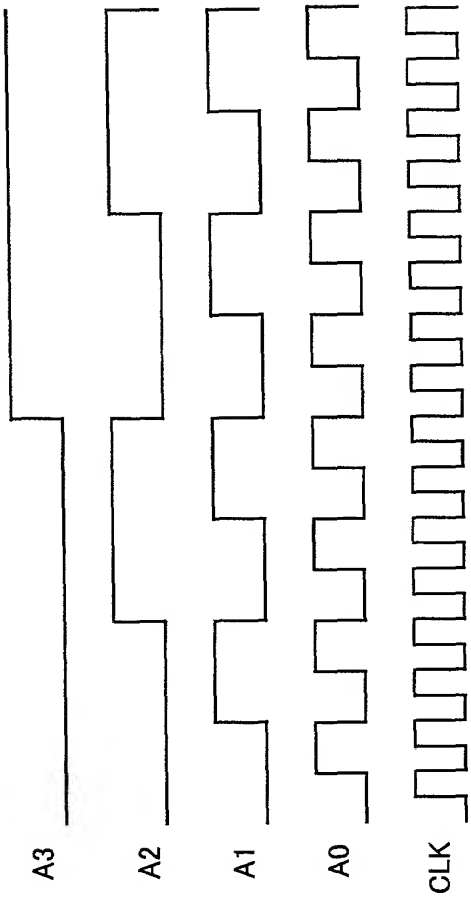


FIG. 12B
(PRIOR ART)

A3	A2	A1	A0	a number of changing bits
0	0	0	0	4
0	0	0	1	1
0	0	1	0	2
0	0	1	1	1
0	1	0	0	3
0	1	0	1	1
0	1	1	0	2
0	1	1	1	1
1	0	0	0	4
1	0	0	1	1
1	0	1	0	2
1	0	1	1	1
1	1	0	0	3
1	1	0	1	1
1	1	1	0	2
1	1	1	1	1
				total 30

FIG. 13
(PRIOR ART)

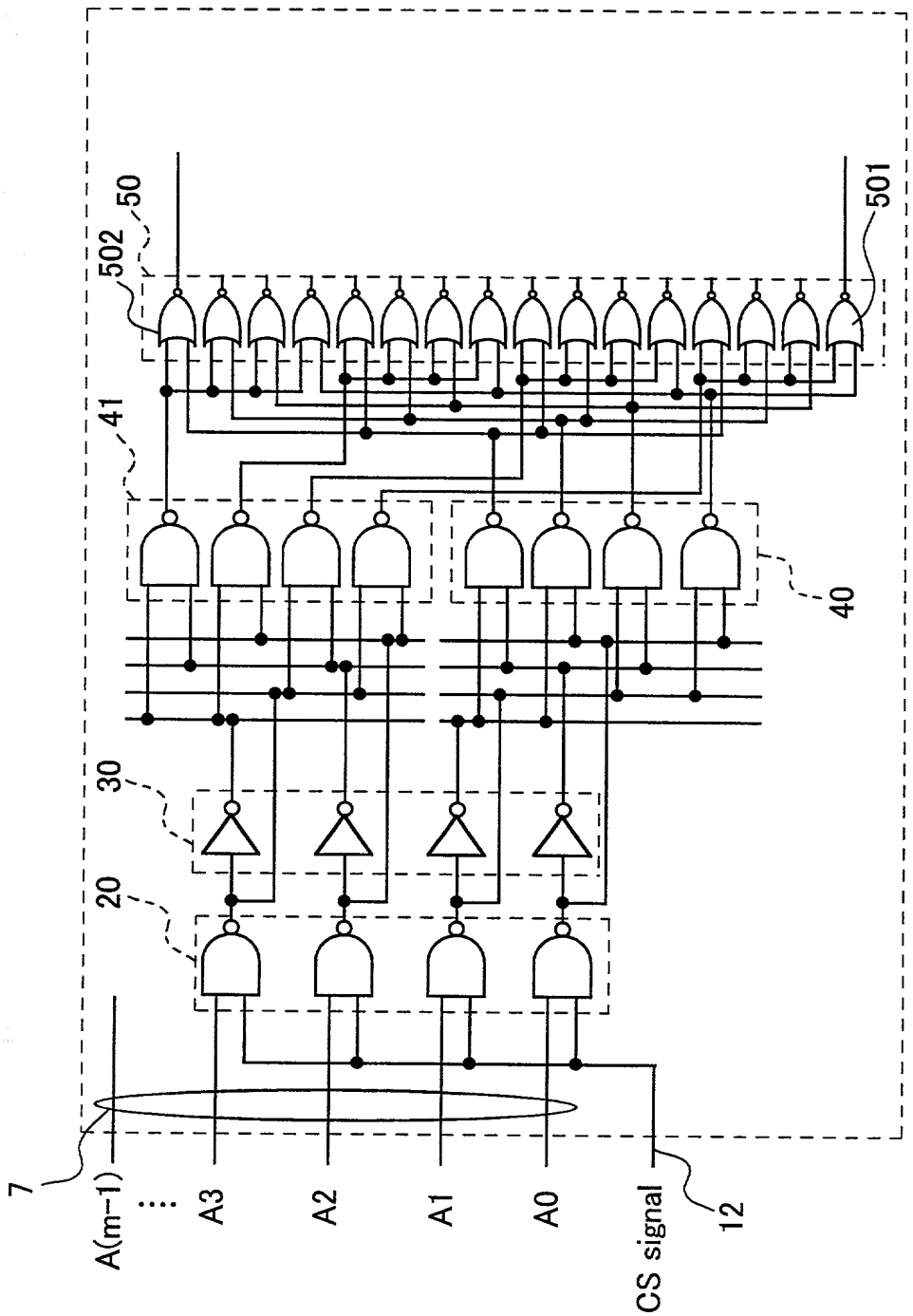


FIG. 14
(PRIOR ART)

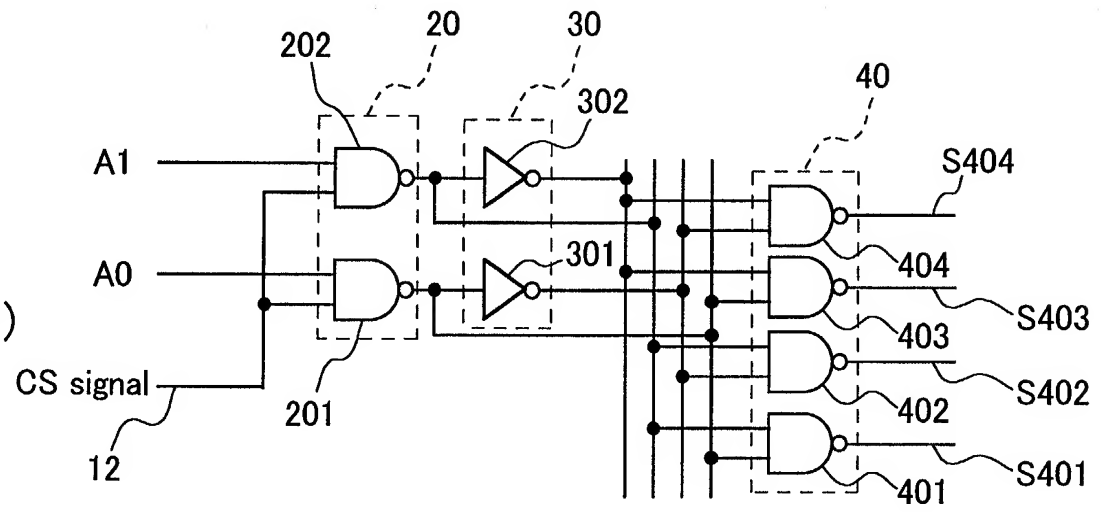


FIG. 15A
(PRIOR ART)

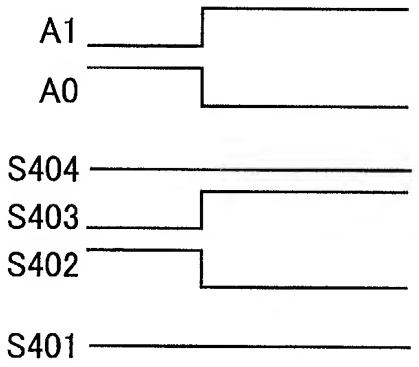


FIG. 15B
(PRIOR ART)

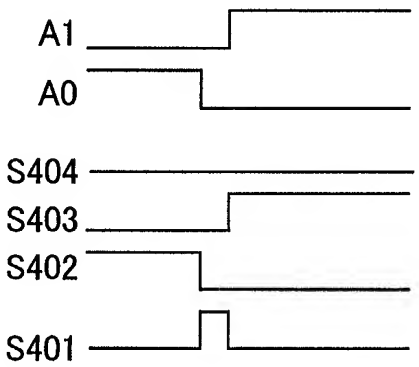


FIG. 15C
(PRIOR ART)

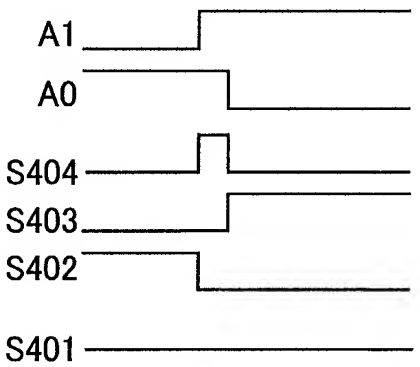


FIG. 15D
(PRIOR ART)